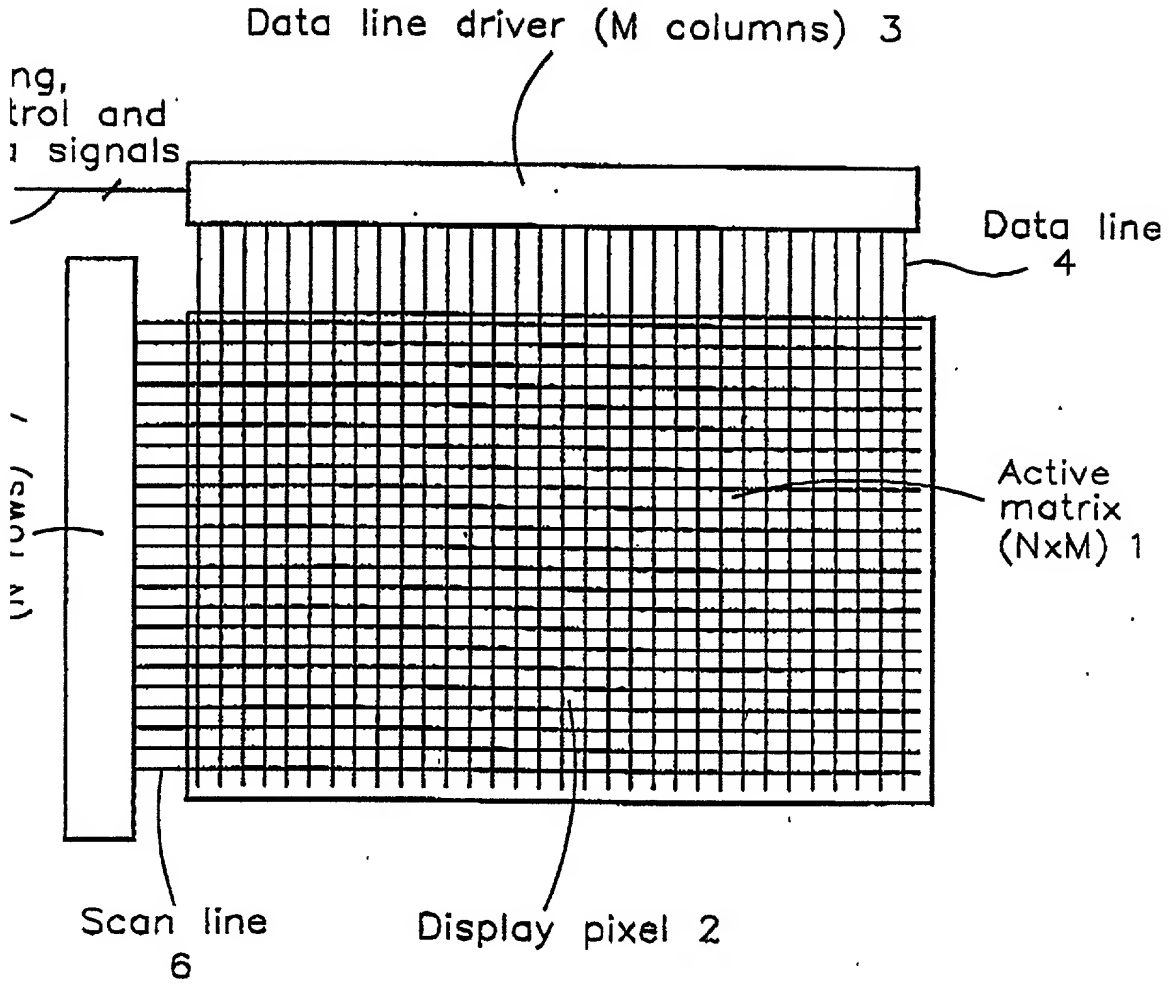

Data line driver (M columns) 3
ng,
trol and
signals
Data line
4
Active
matrix
(NxM) 1
Scan line
6
Display pixel 2

FIG 1

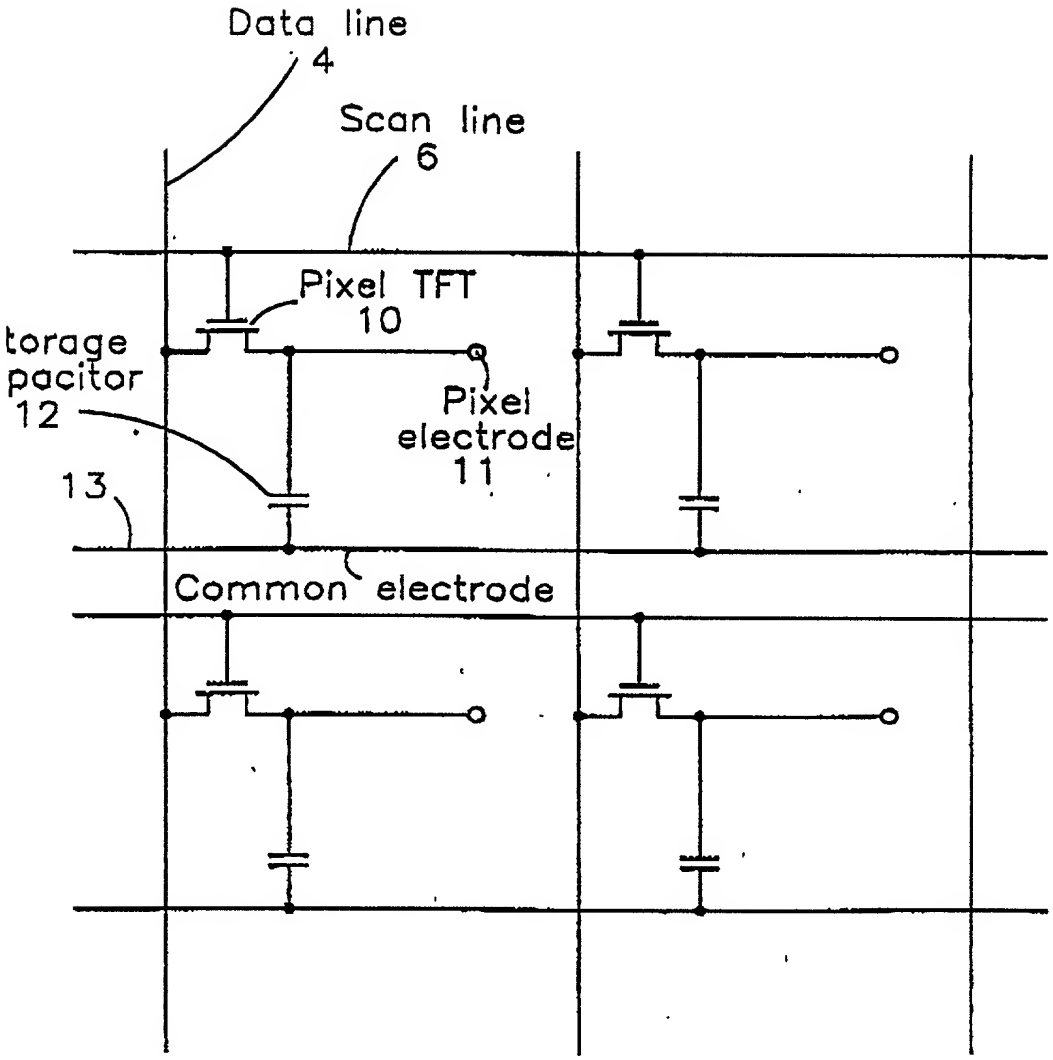

Data line
4
Scan line
6
Pixel TFT
10
torage
pacitor
12
Pixel
electrode
11
13
Common electrode

FIG 2

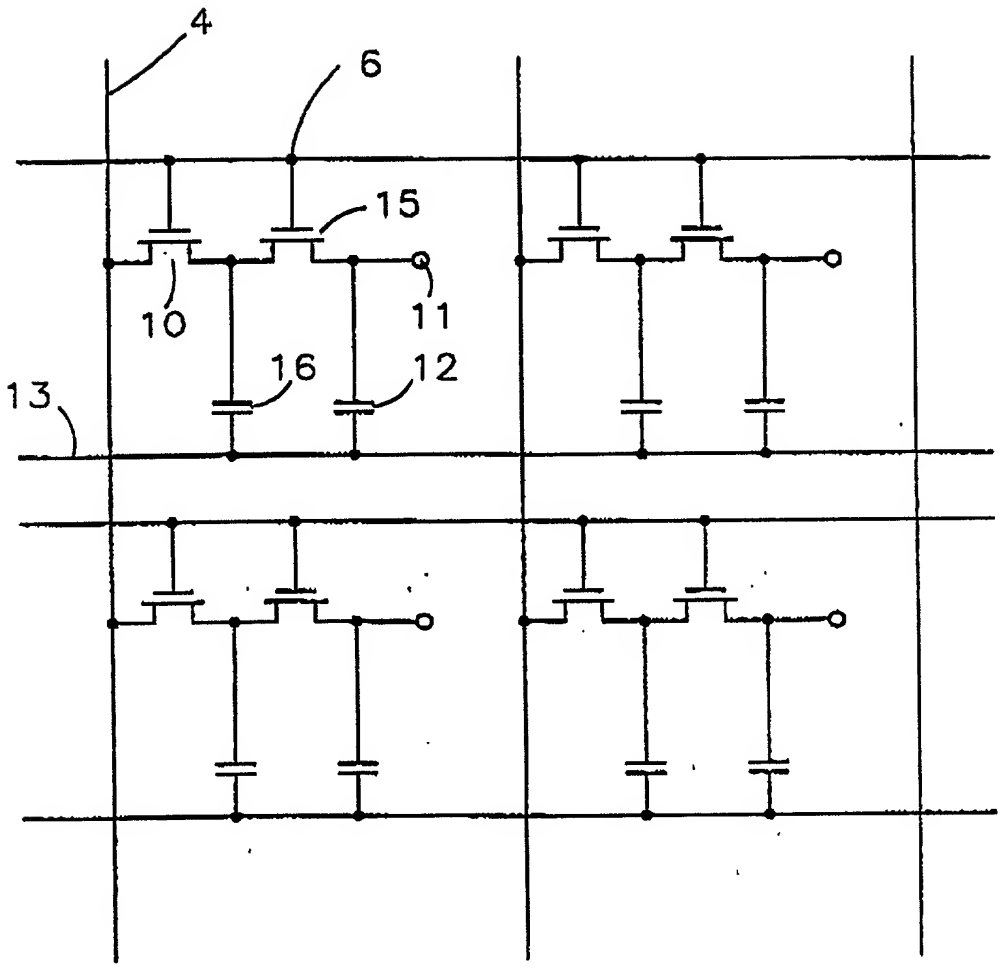


FIG 3

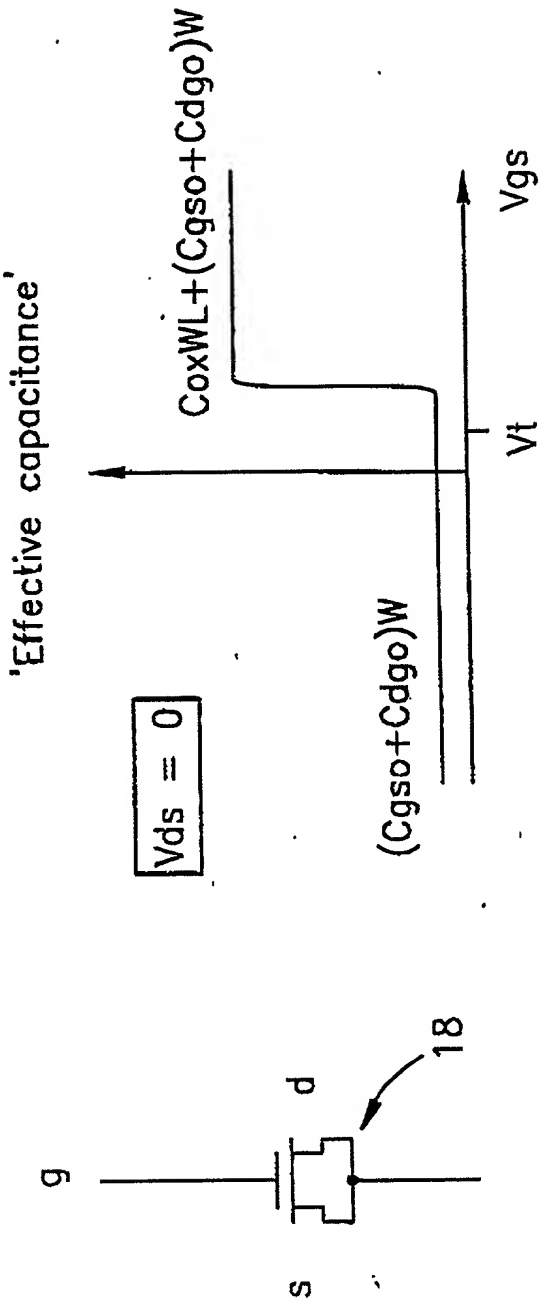

'Effective capacitance'
CoxWL+(Cgso+Cdgo)W
Vds = 0
Vt
Vgs
(Cgso+Cdgo)W
g
d
s
18

FIG 4

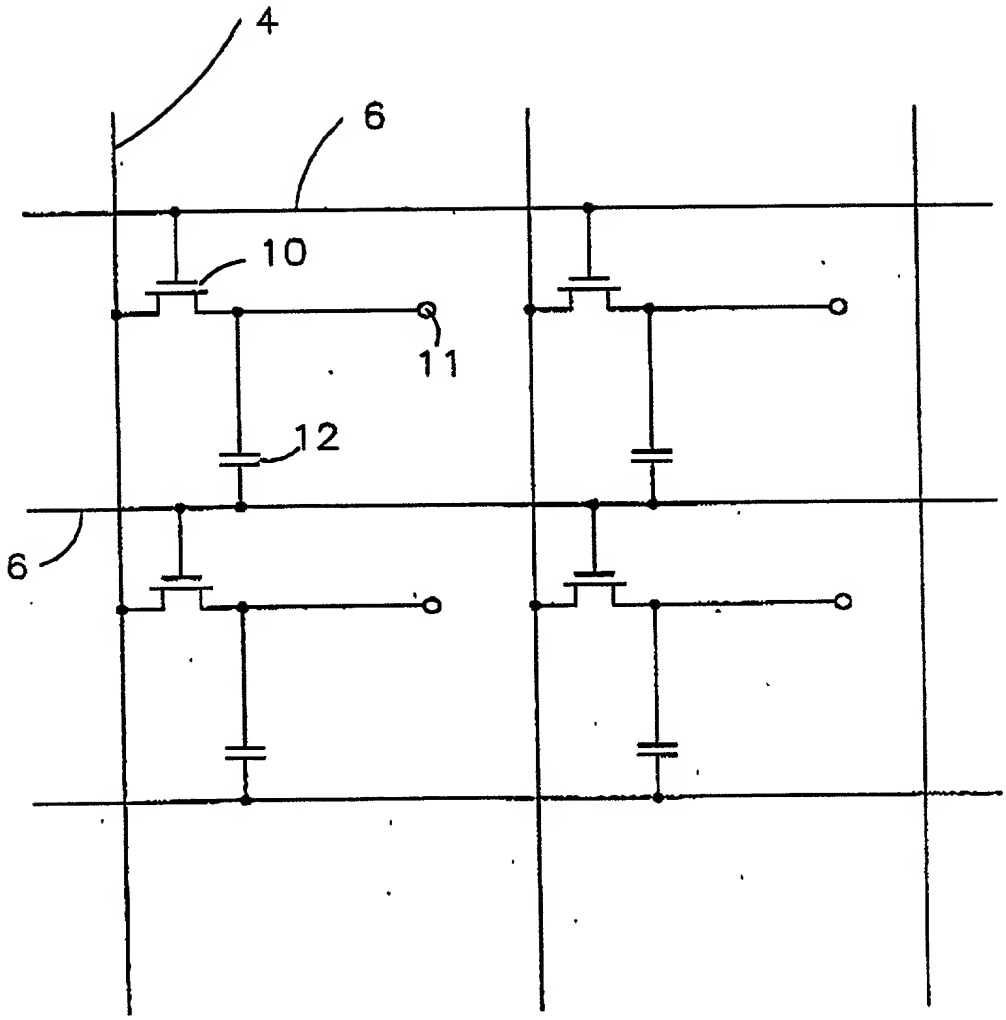


FIG 5

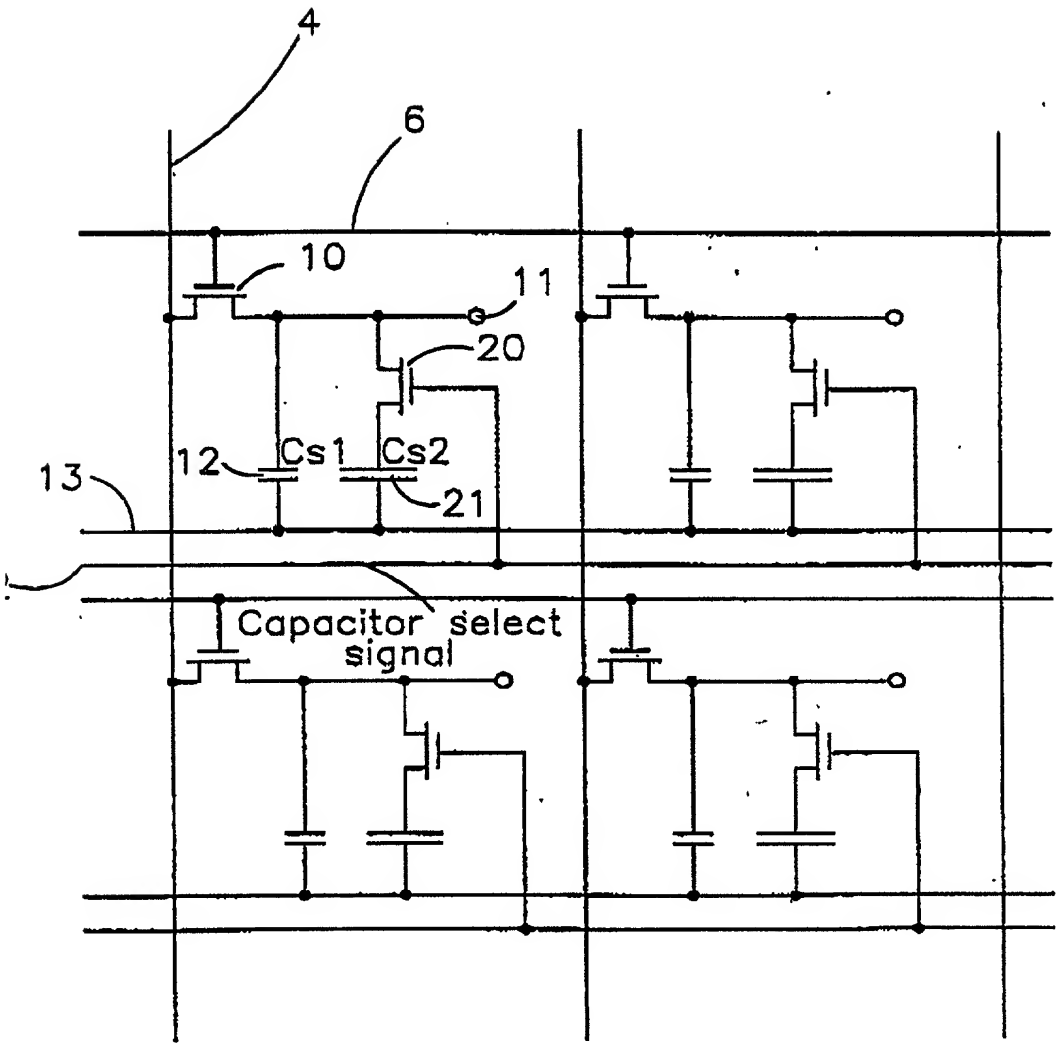


FIG 6

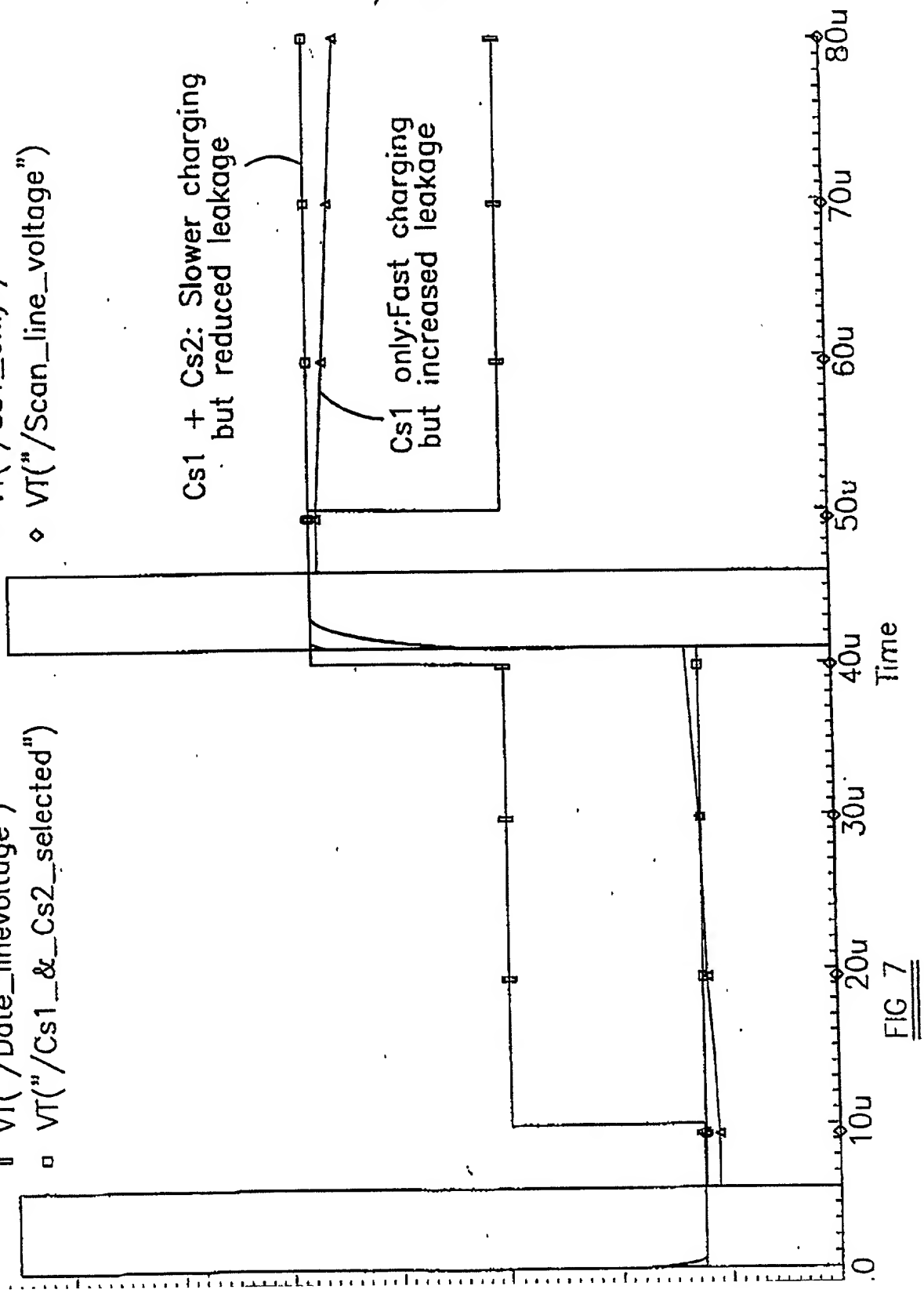

V(/Gate_linevoltage)
VT("/Cs1_&_Cs2_selected")
V(/Cs1_only)
VT("/Scan_line_voltage")
Cs1 + Cs2: Slower charging
but reduced leakage
Cs1 only:Fast charging
but increased leakage
0
10u
20u
30u
40u
50u
60u
70u
80u
Time

FIG 7

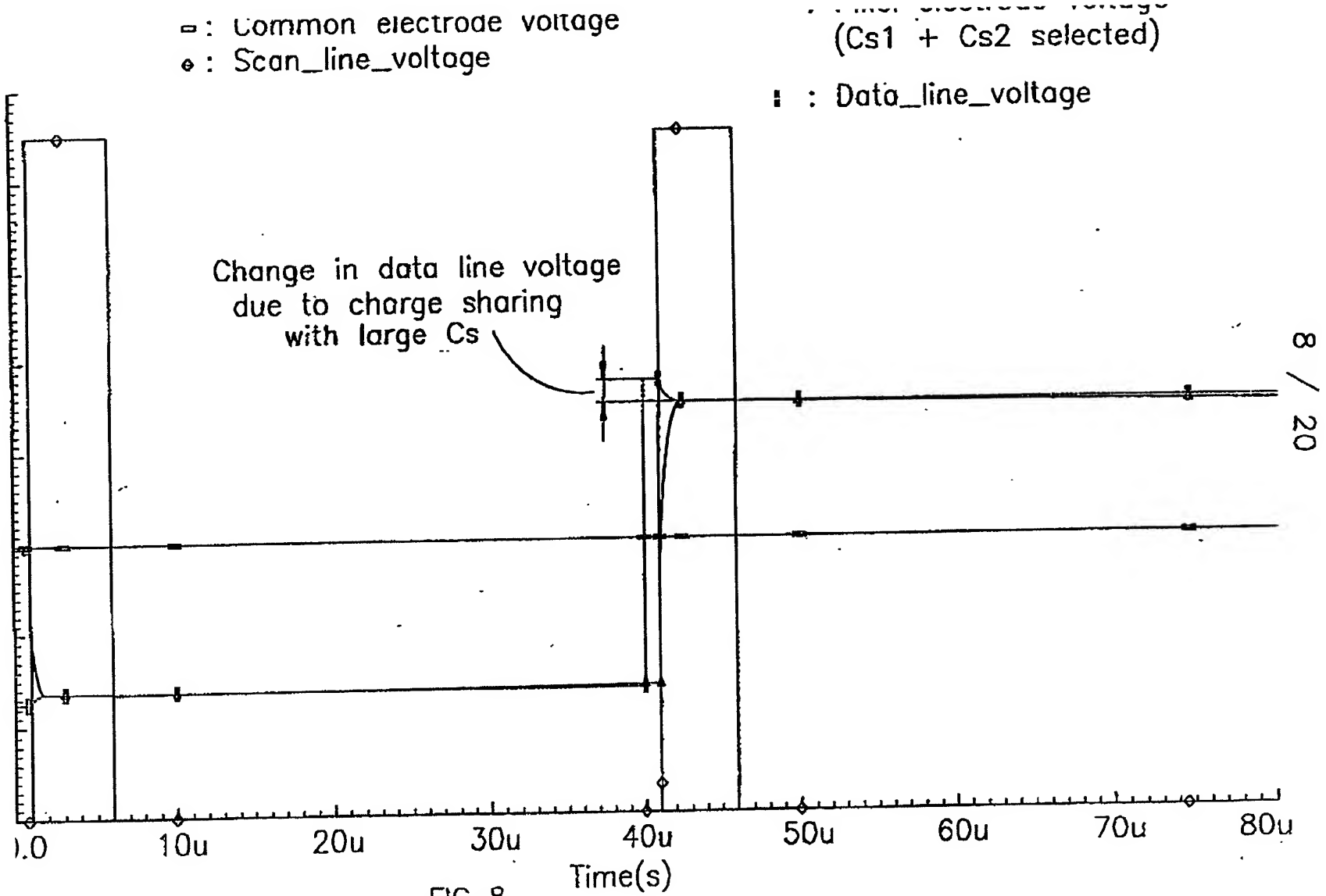


FIG 8

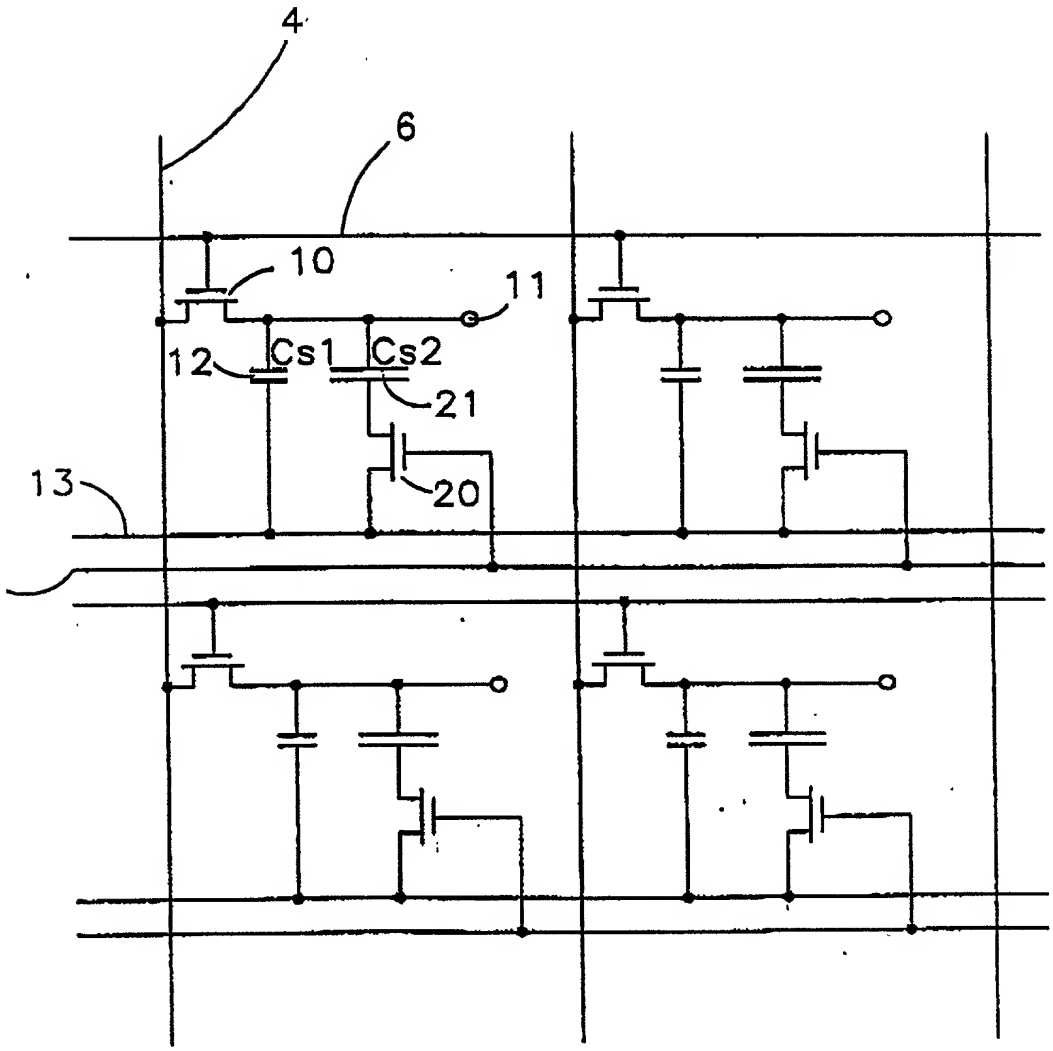


FIG 9

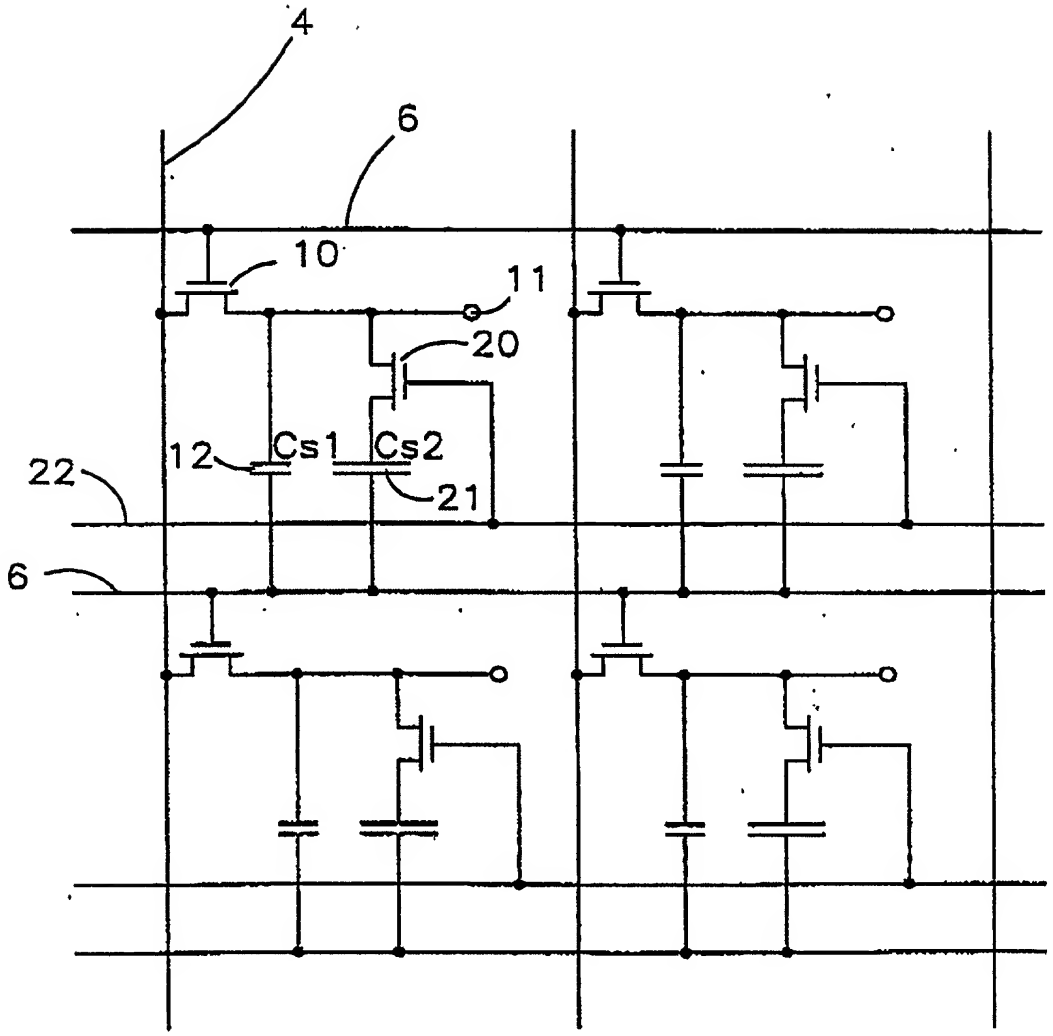


FIG 10

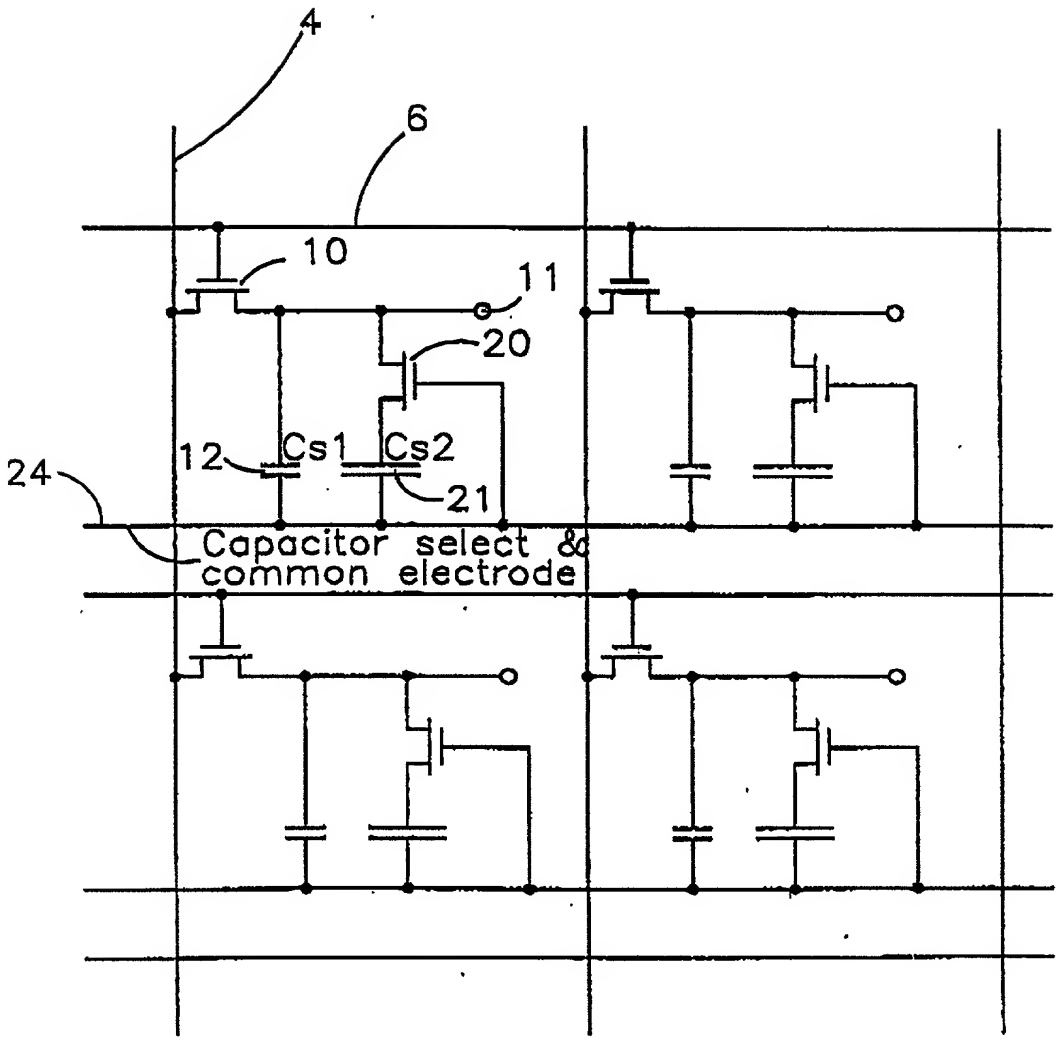

4
6
10
11
20
12
Cs1
Cs2
21
24
Capacitor select &
common electrode

FIG 11

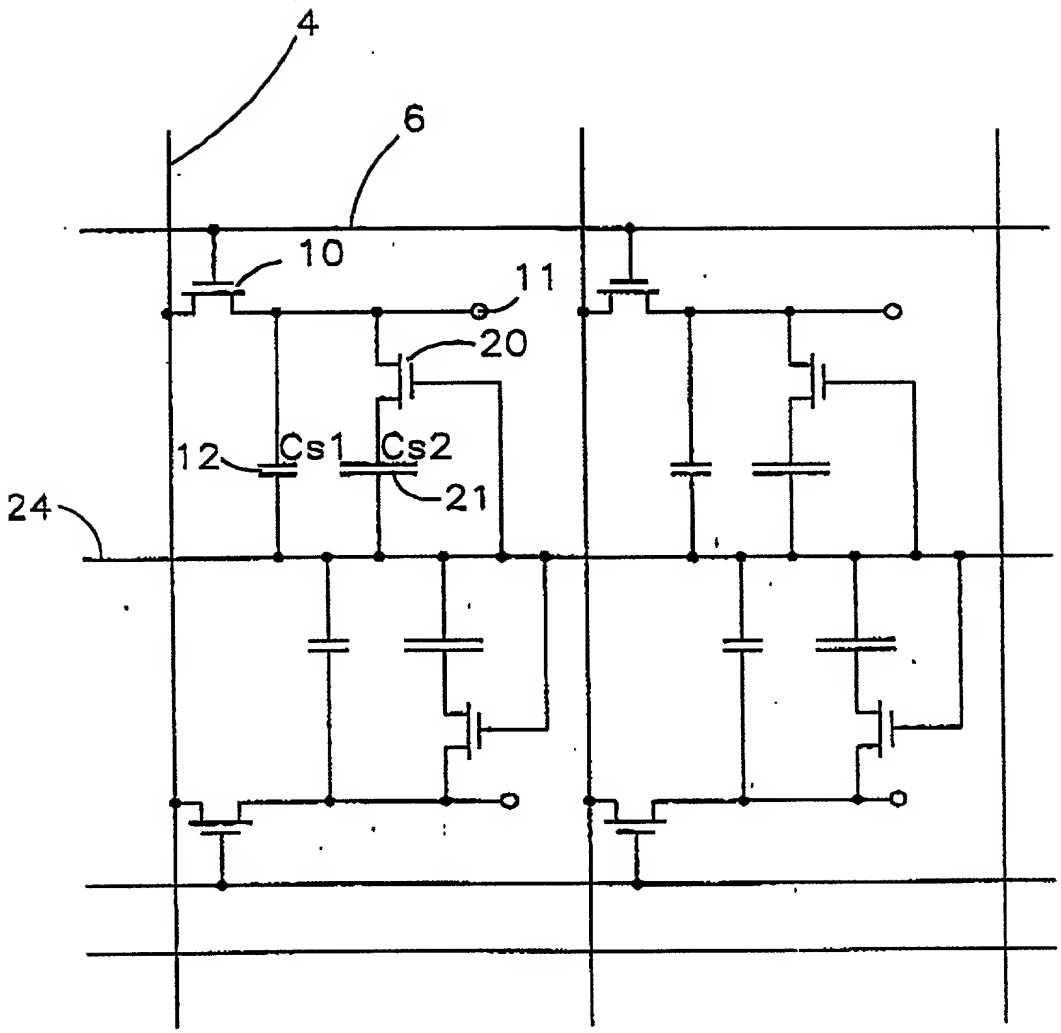


FIG 12

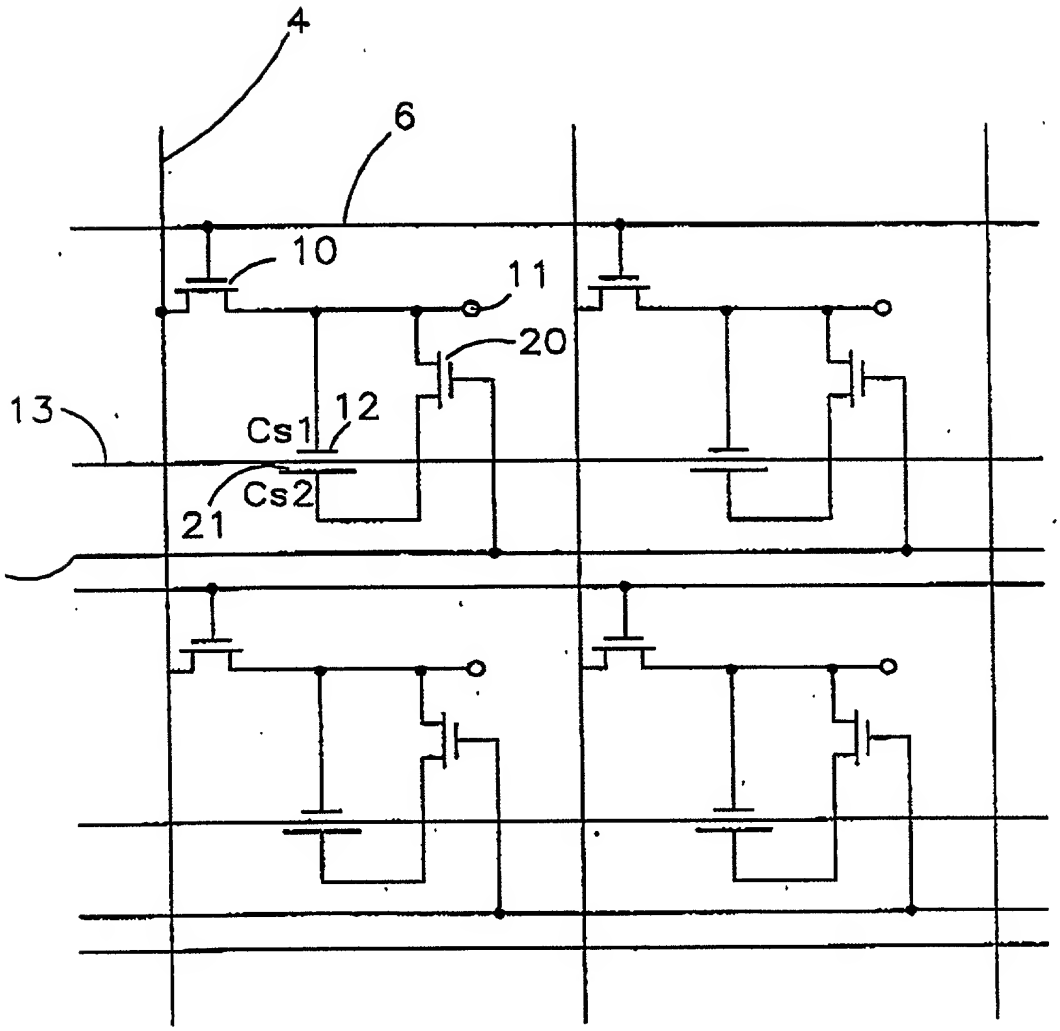


FIG 13

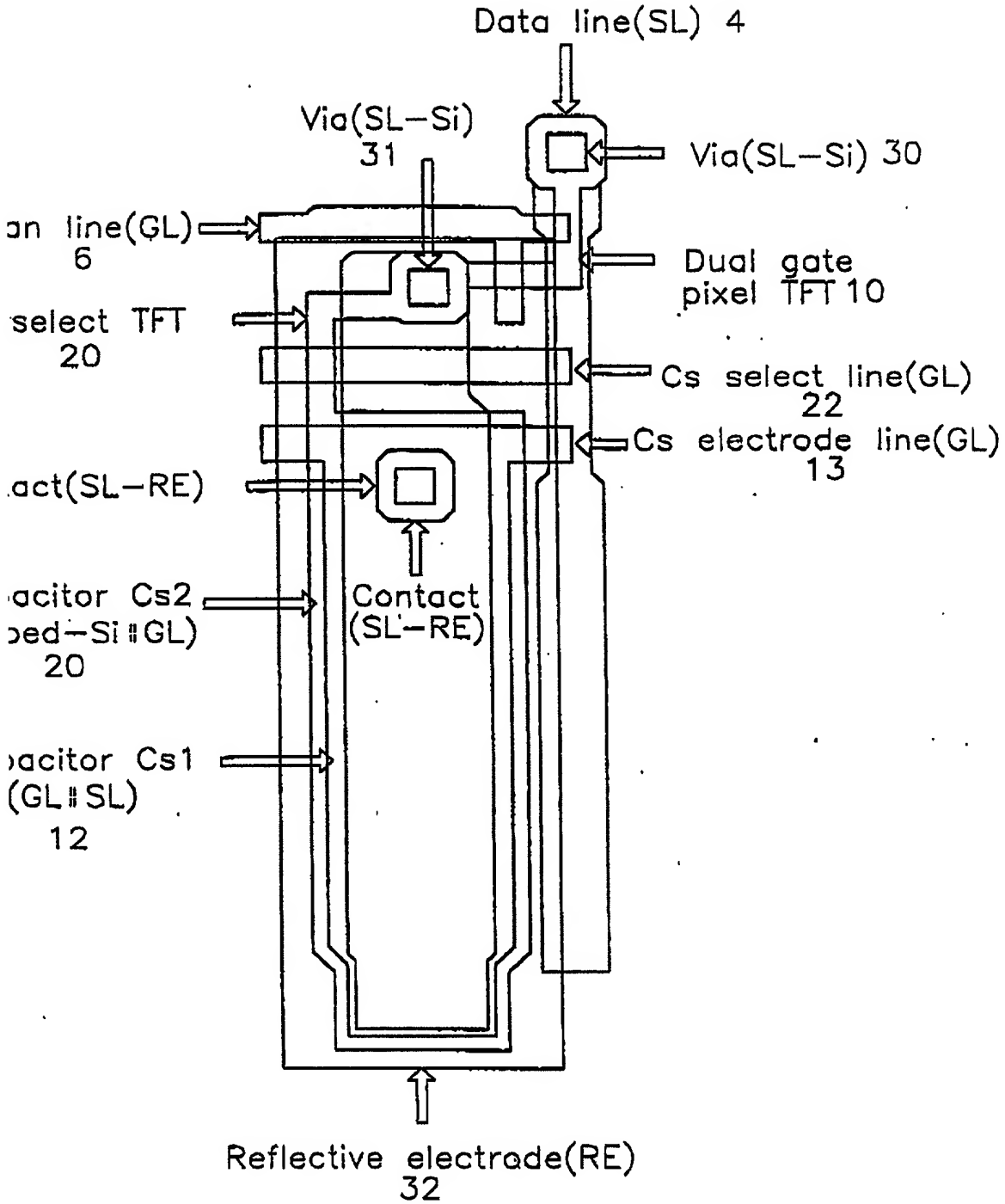

Data line(SL) 4
Via(SL-Si)
31
Via(SL-Si) 30
an line(GL)
6
Dual gate
pixel TFT 10
select TFT
20
Cs select line(GL)
22
Cs electrode line(GL)
13
act(SL-RE)
Contact
(SL-RE)
acitor Cs2
ed-Si GL)
20
acitor Cs1
(GL SL)
12
Reflective electrode(RE)
32

FIG. 14

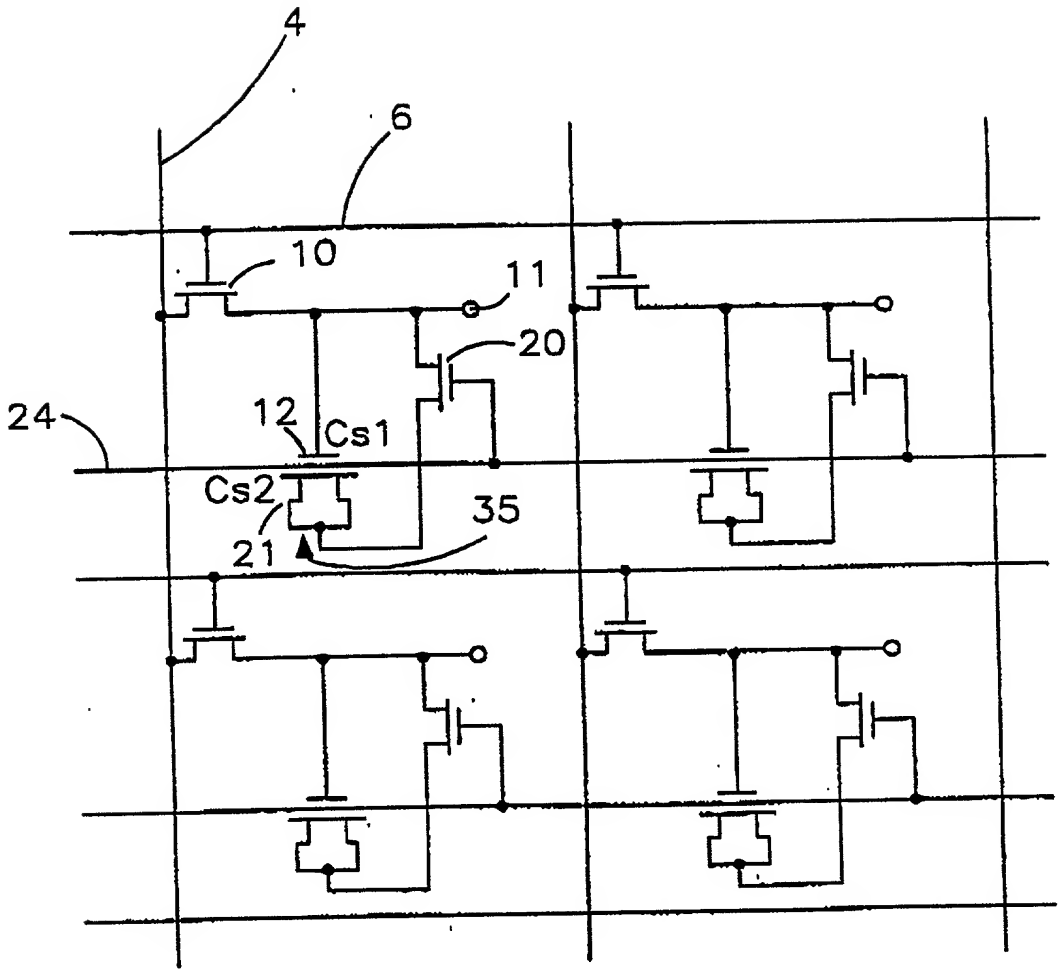


FIG 15

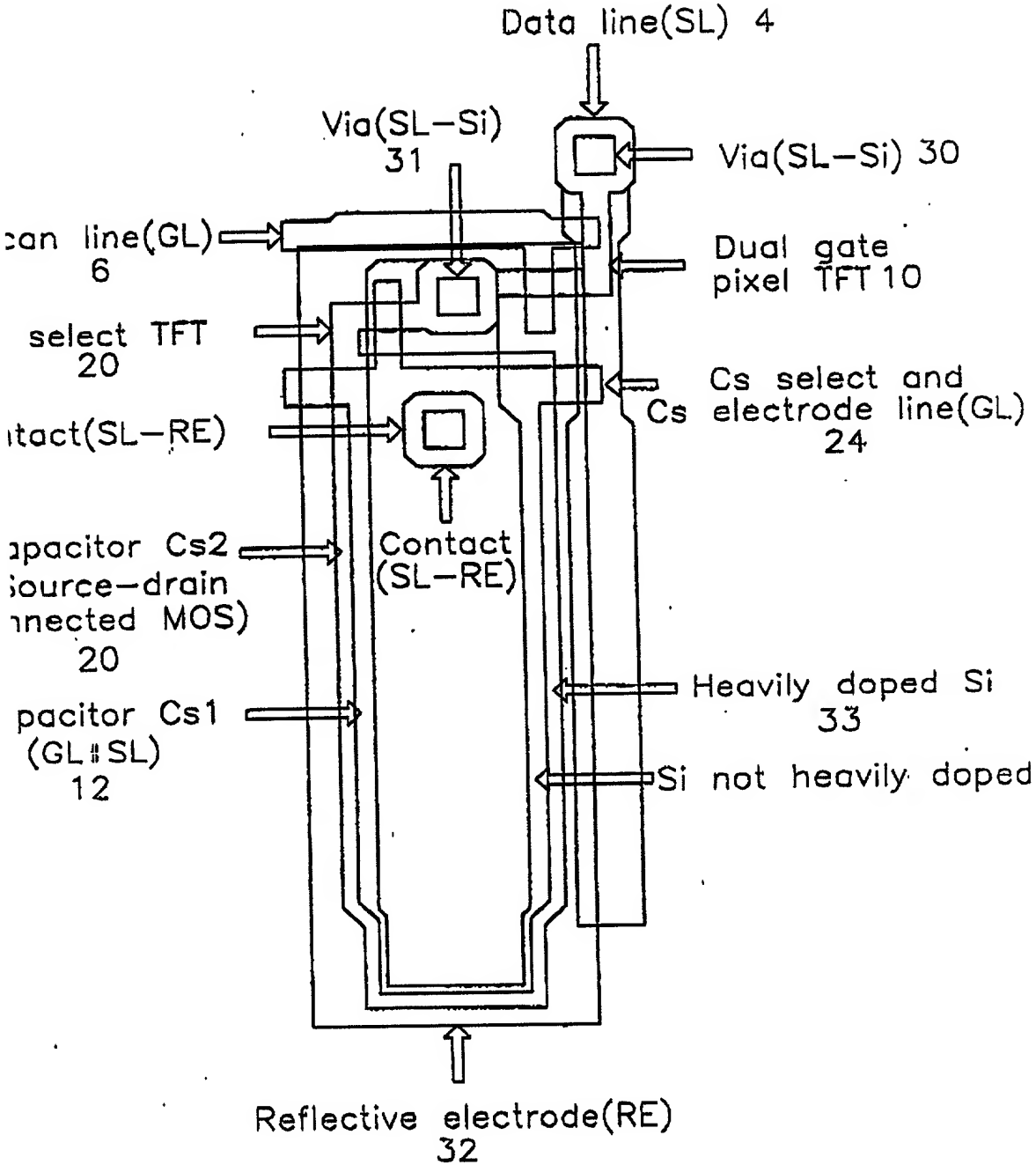
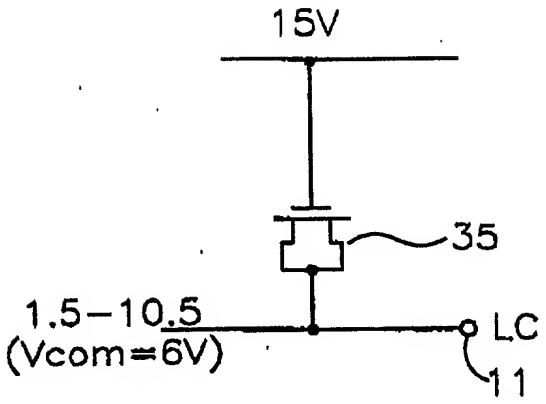
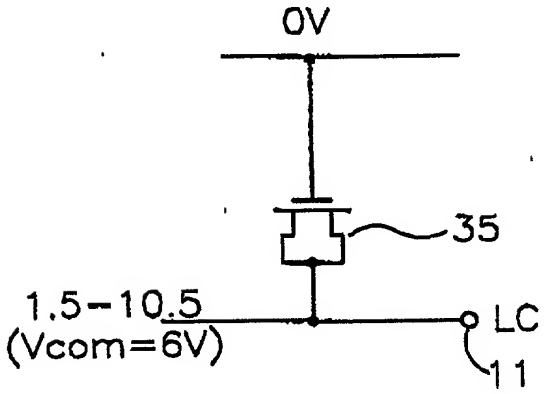

Data line(SL) 4
Via(SL–Si)
31
Via(SL–Si) 30
can line(GL)
6
Dual gate
pixel TFT 10
select TFT
20
Cs select and
Cs electrode line(GL)
24
ntact(SL–RE)
Contact
(SL–RE)
apacitor Cs2
source–drain
nnected MOS)
20
Heavily doped Si
33
pacitor Cs1
(GL‖SL)
12
Si not heavily doped
Reflective electrode(RE)
32

FIG. 16



Condition for
high capacitance:
Vt<4.5



Condition for
low capacitance:
Vt>–1.5

FIG 17

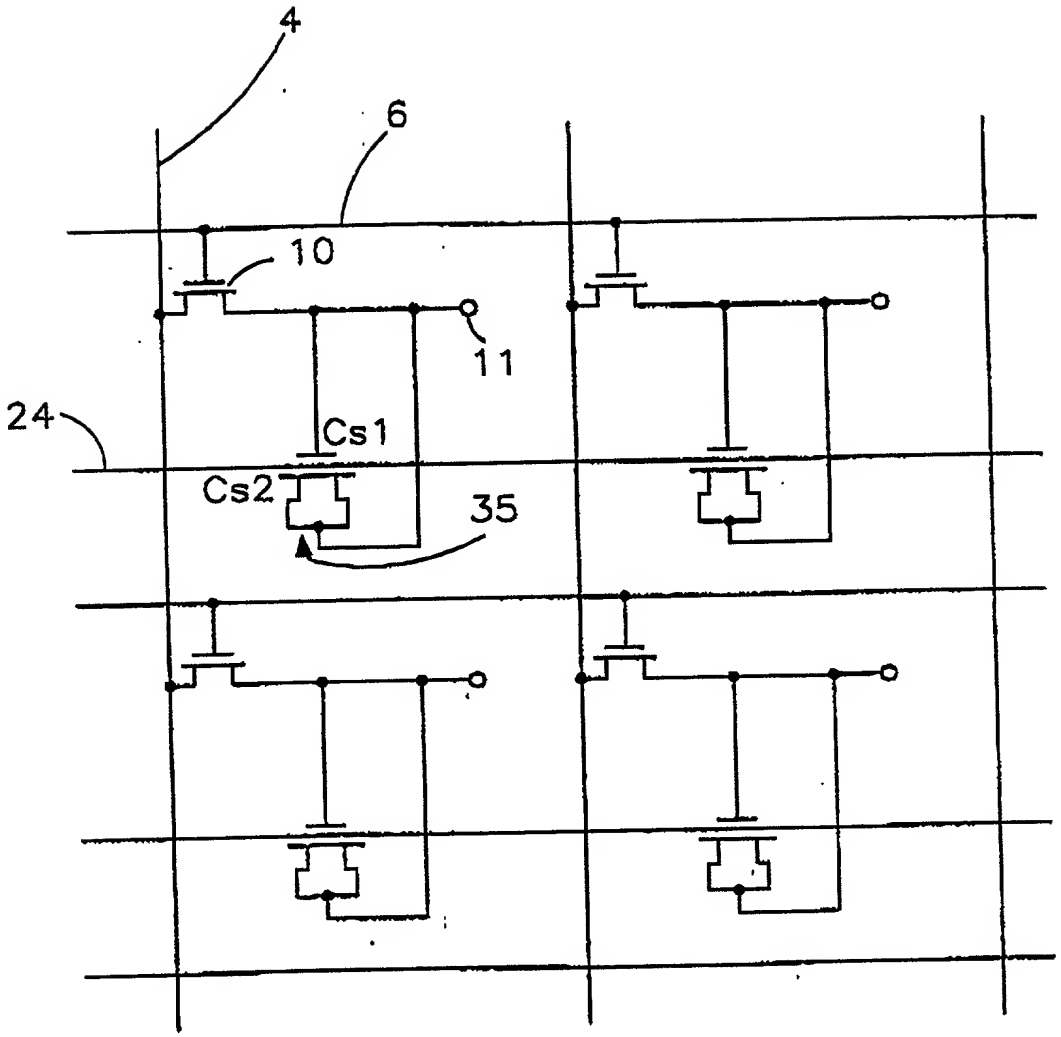


FIG 18

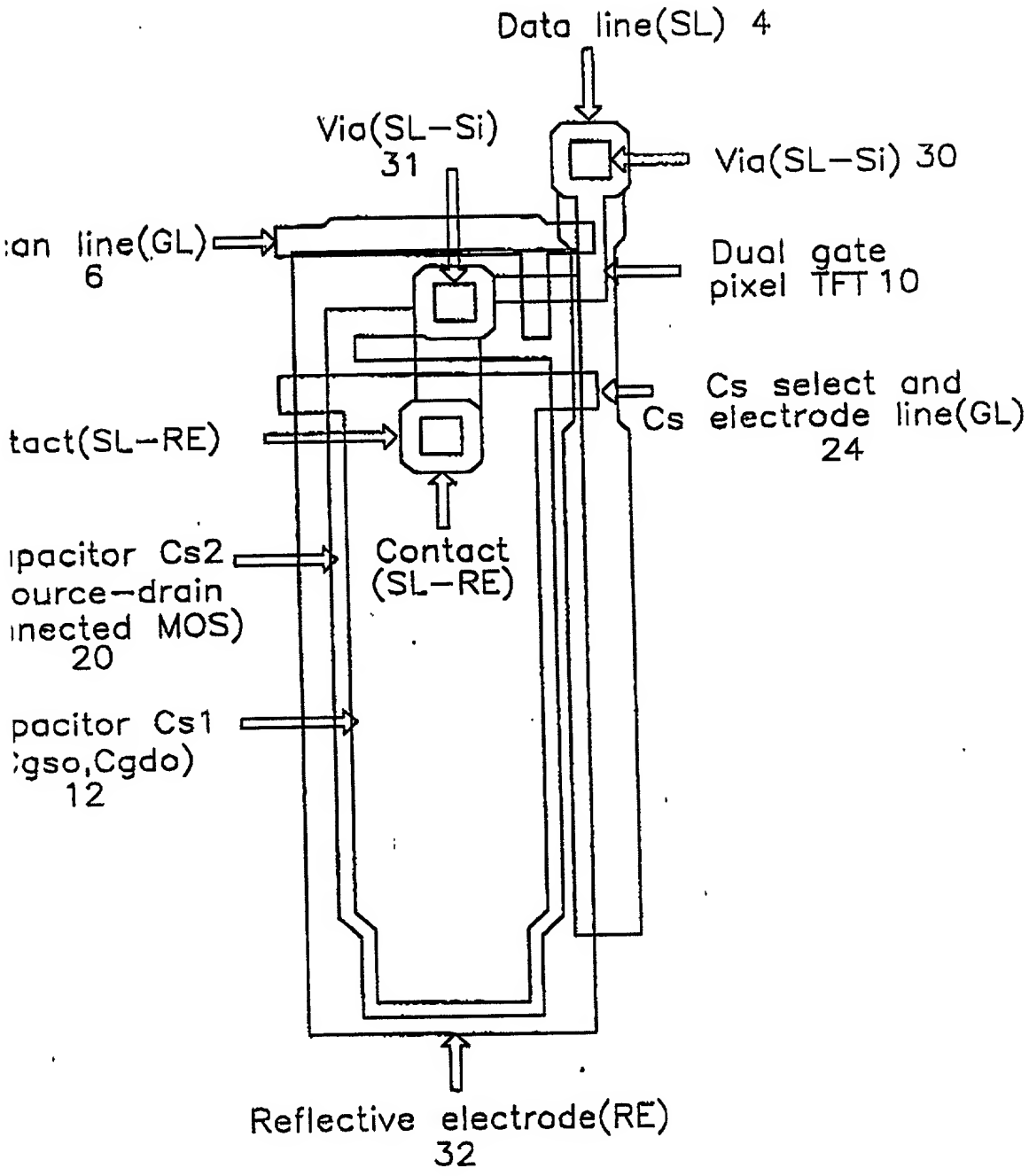

Data line(SL) 4
Via(SL-Si) 31
Via(SL-Si) 30
an line(GL) 6
Dual gate pixel TFT 10
Cs select and Cs electrode line(GL) 24
tact(SL-RE)
Contact (SL-RE)
pacitor Cs2
ource-drain
nected MOS) 20
pacitor Cs1
gso,Cgdo) 12
Reflective electrode(RE) 32

FIG. 19

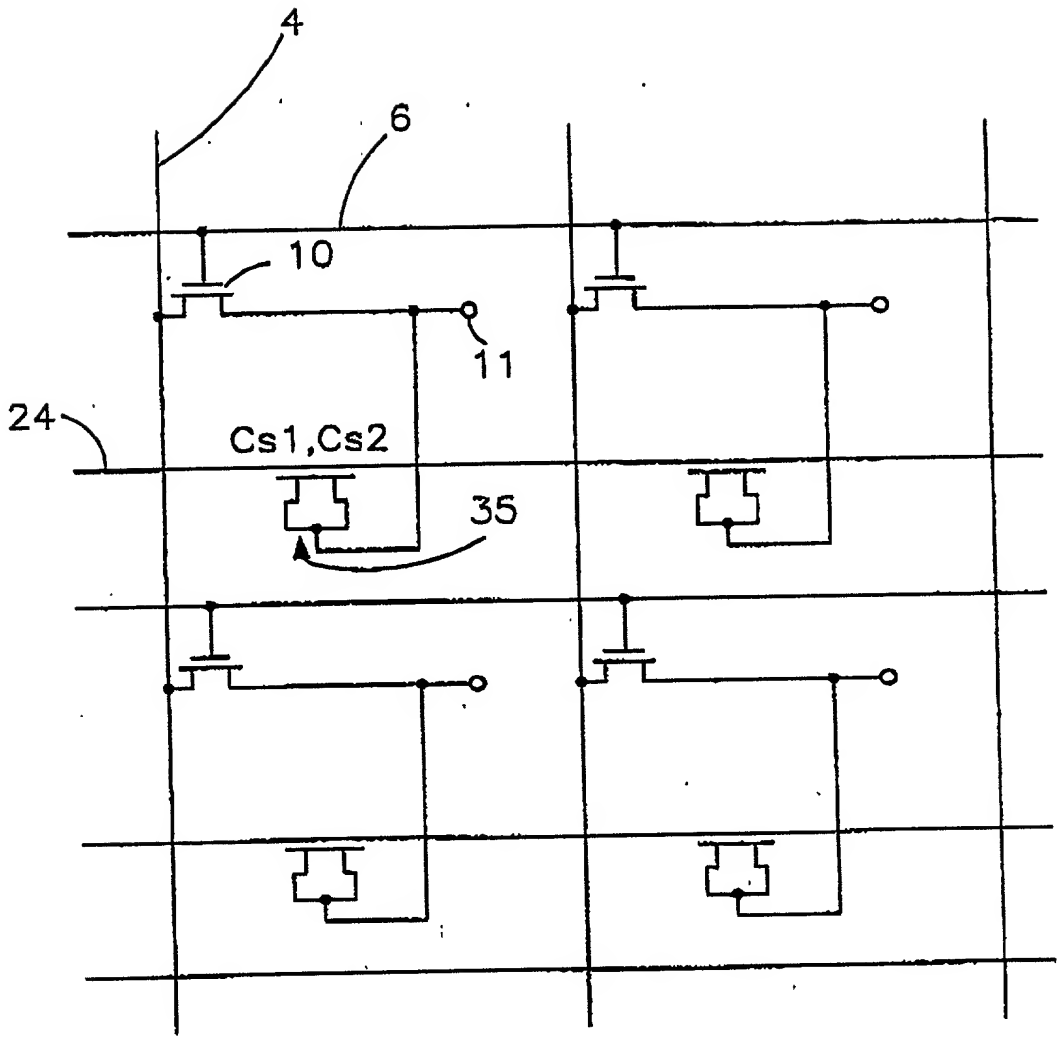


FIG 20